

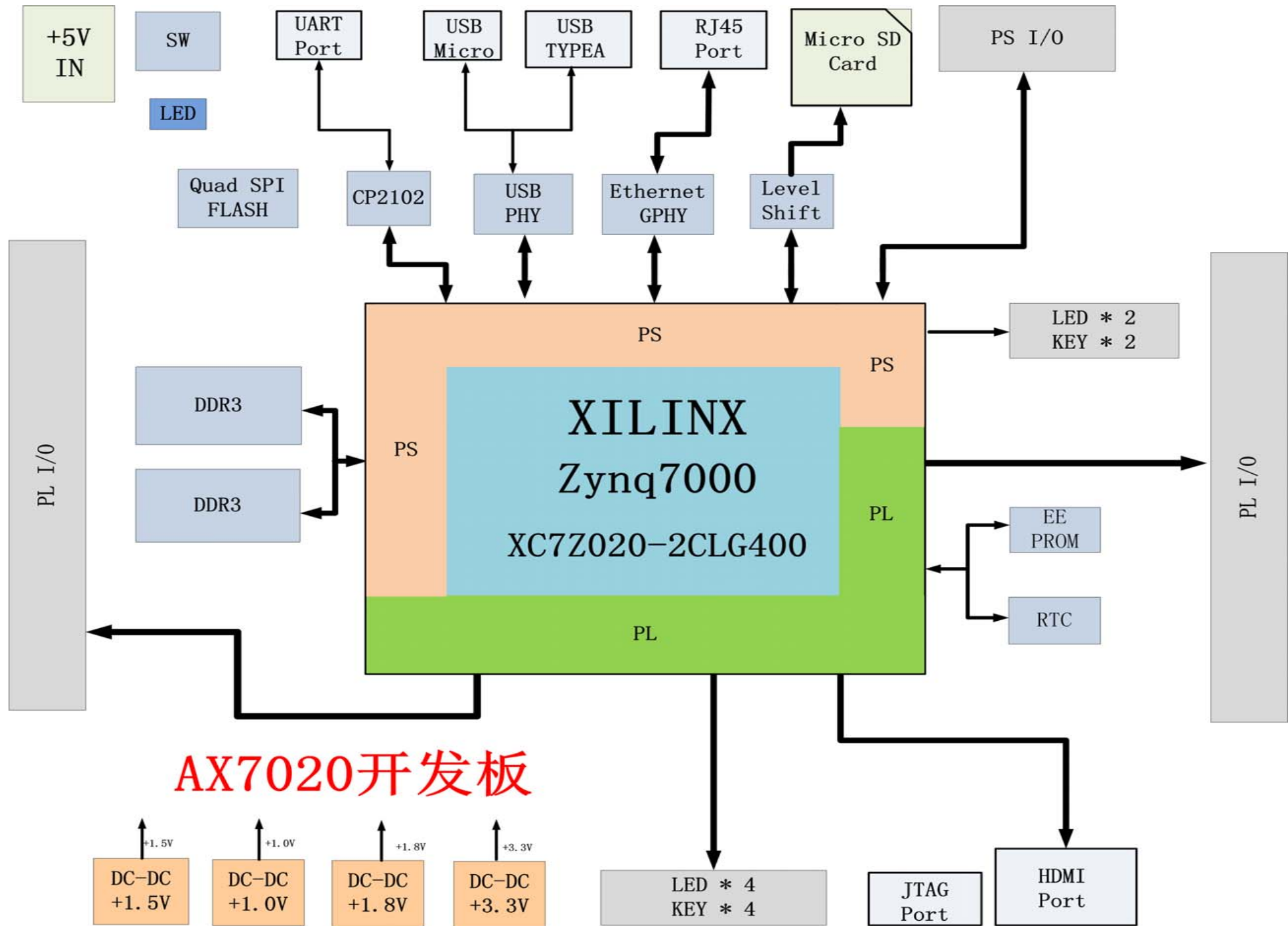
REV	Description	Date
V1.0	First Release	2016-7-12

AX7010/AX7020 Schematics

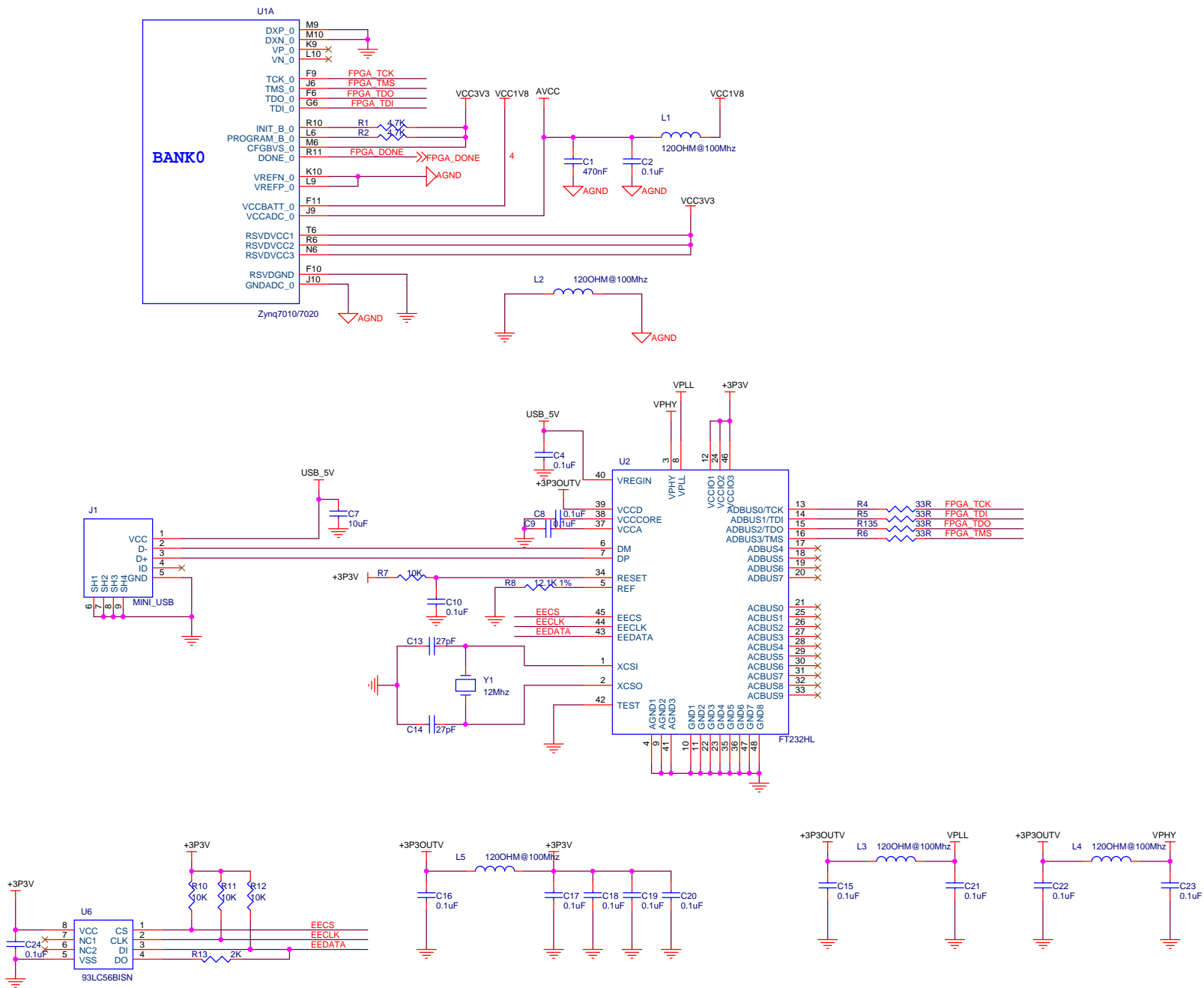
黑金ZYNQ硬件平台

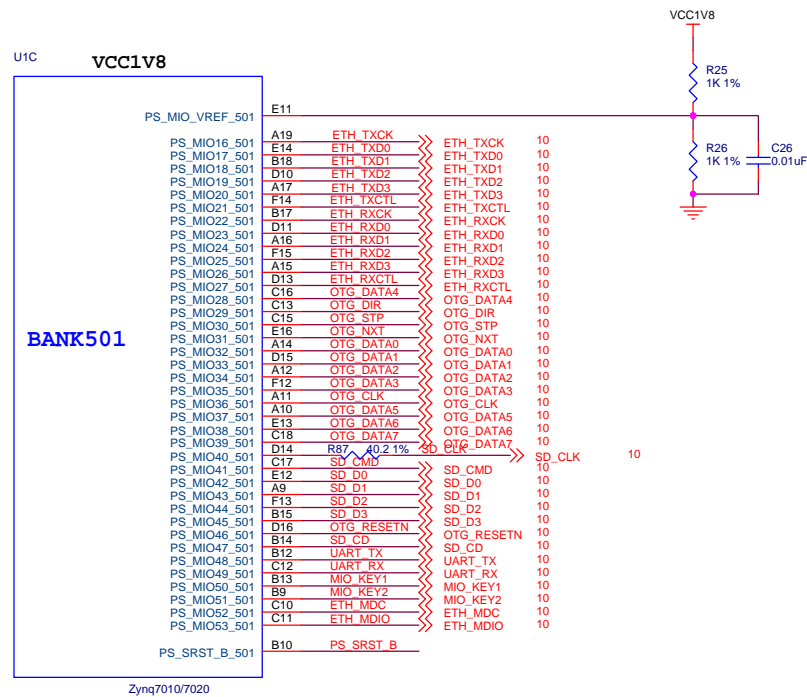
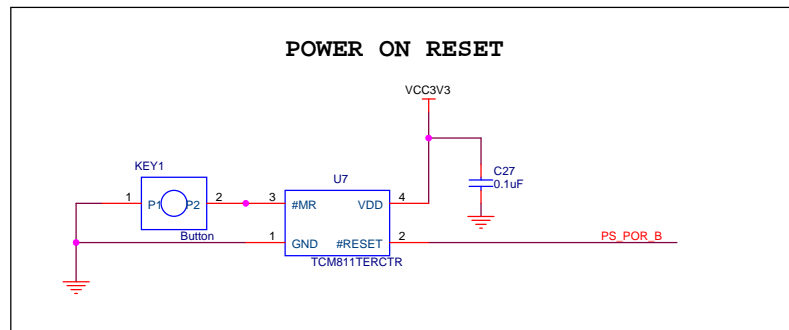
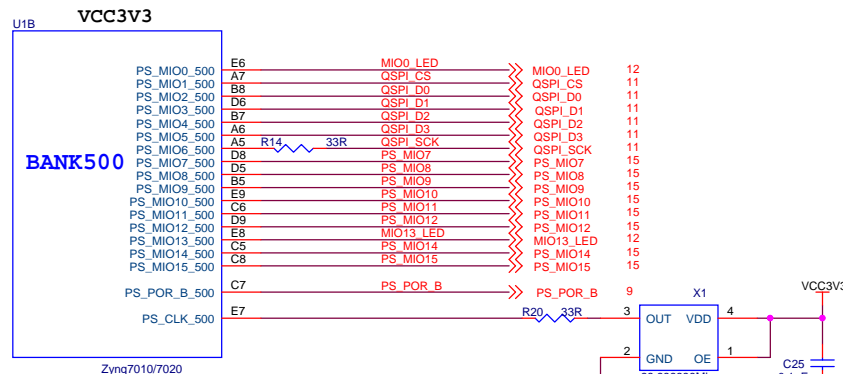
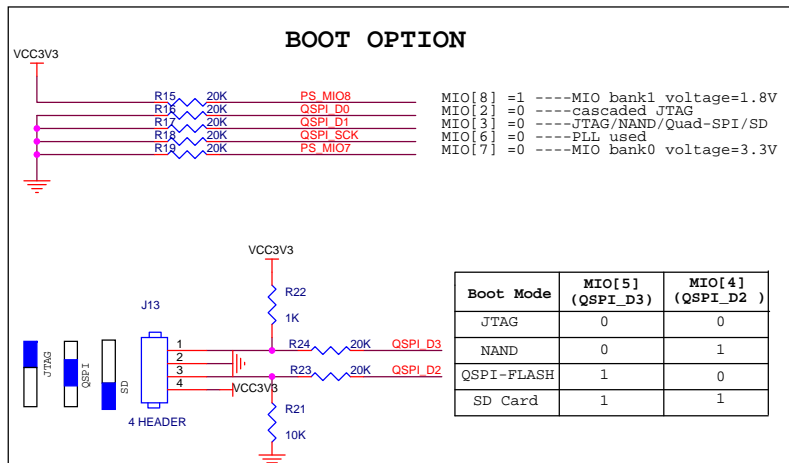
Page Number	Description
Page01	Cover Page
Page02	Block Diagram
Page03	Zynq-7000 JTAG & Bank0
Page04	Zynq-7000 MIO Config
Page05	Zynq-7000 Bank13-34-35
Page06	Zynq-7000 Bank502
Page07	Zynq-7000 Power
Page08	DDR3
Page09	GPHY
Page10	USB OTG
Page11	FLASH, RTC, EEPROM
Page12	LED, KEY
Page13	UART, SD
Page14	HDMI
Page15	EXTEND IO
Page16	POWER

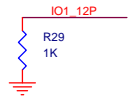
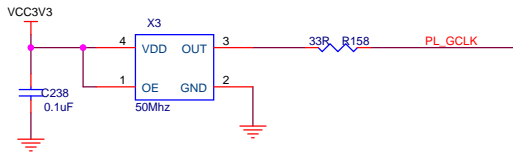
ALINX		
Title Zynq-7000 Cover Page		
Size	Document Number AX7010/AX7020开发板原理图	Rev 1.0
Date:	Monday, October 08, 2018	Sheet 1 of 16



AX7020开发板

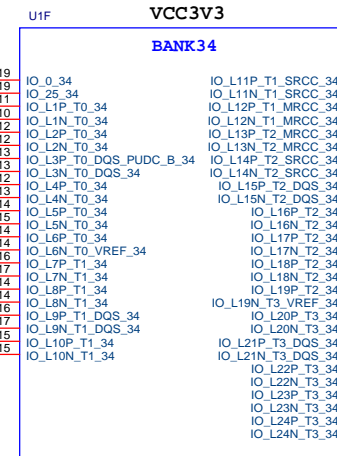




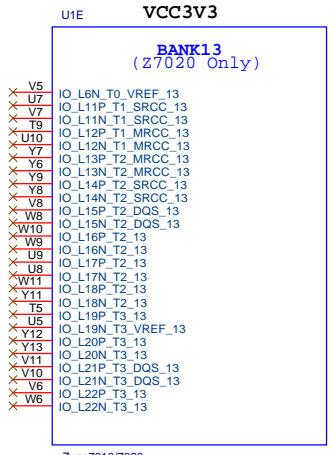


- 11 RTC_SCLK
- 11 EEPROM_I2C_SCL
- 15 IO1_15P
- 15 IO1_15N
- 15 IO1_14P
- 15 IO1_14N
- 15 IO1_12P
- 15 IO1_12N
- 15 IO1_13P
- 15 IO1_13N
- 15 IO1_11P
- 15 IO1_11N
- 15 IO1_2P
- 15 IO1_2N
- 15 IO1_3P
- 15 IO1_3N
- 15 IO1_5P
- 15 IO1_5N
- 15 IO1_9P
- 15 IO1_9N
- 15 IO1_4P
- 15 IO1_4N

- R19
- T19
- T11
- T10
- T12
- U12
- U13
- V13
- V12
- W13
- T14
- T15
- P14
- R14
- Y16
- Y17
- W14
- Y14
- T16
- U17
- V15
- W15



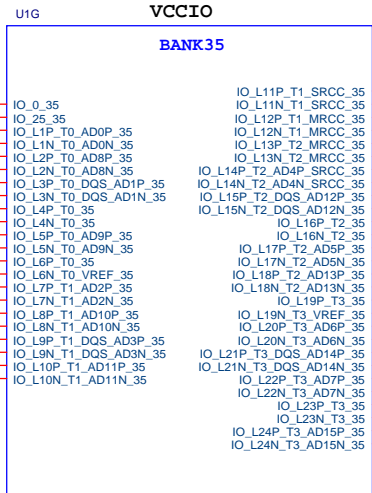
Zynq7010/7020



Zynq7010/7020

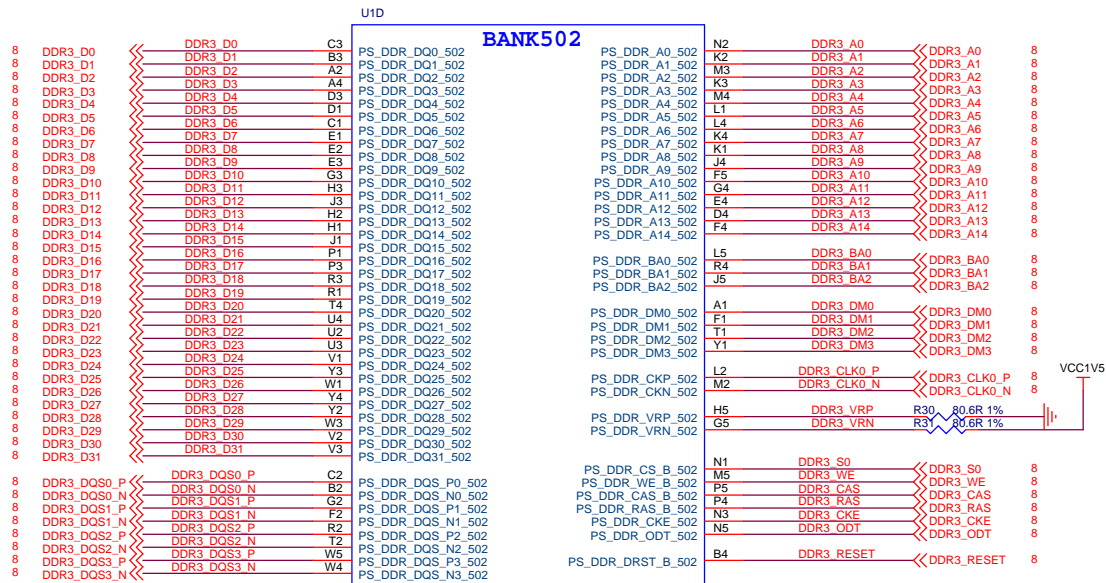
- 15 IO1_17P
- 15 IO1_17N
- 15 IO1_16P
- 15 IO1_16N
- 15 IO2_12P
- 15 IO2_12N
- 15 IO2_13P
- 15 IO2_13N
- 15 IO2_11P
- 15 IO2_11N
- 15 IO2_6P
- 15 IO2_6N
- 15 IO2_11P
- 15 IO2_11N
- 15 IO2_5P
- 15 IO2_5N
- 15 IO2_8P
- 15 IO2_8N

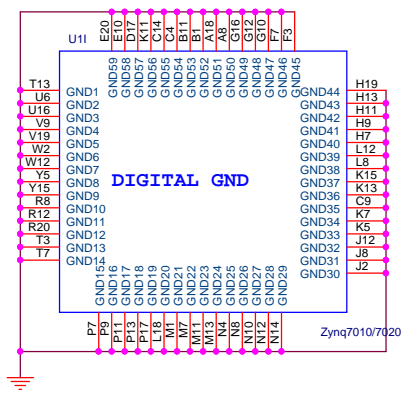
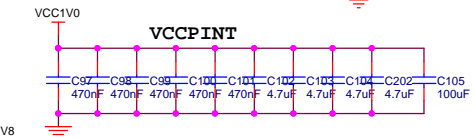
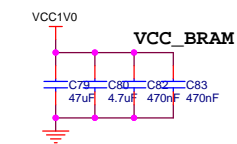
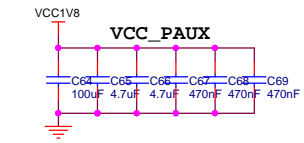
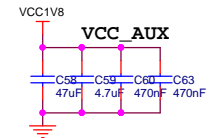
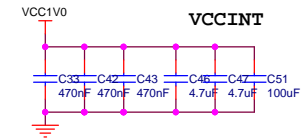
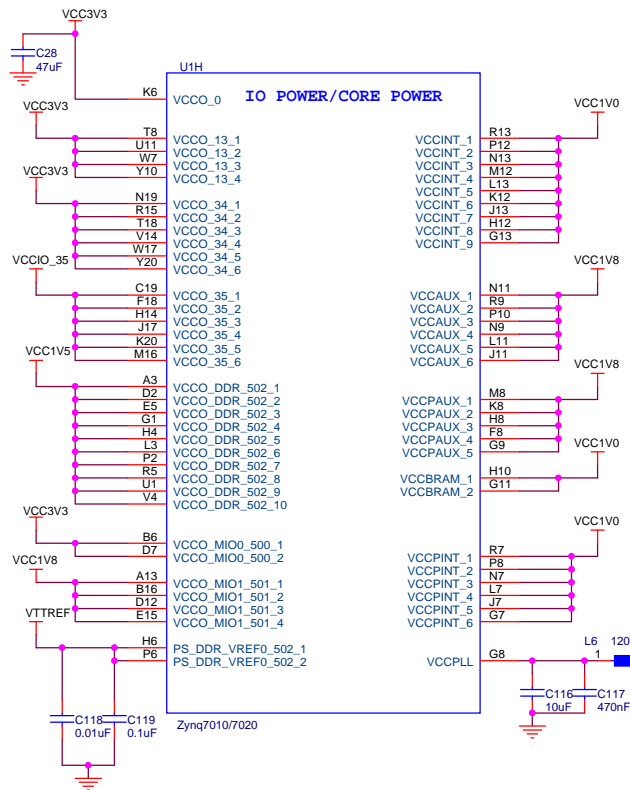
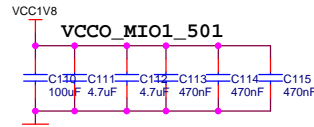
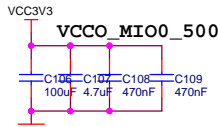
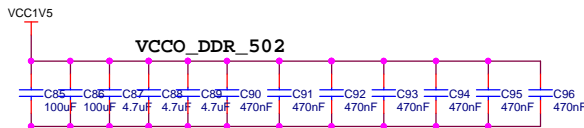
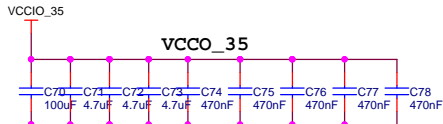
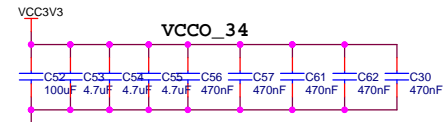
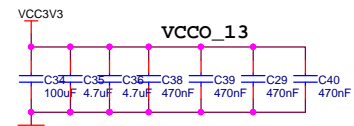
- G14
- J15
- C20
- B20
- B19
- A20
- E17
- D18
- D19
- D20
- E18
- E19
- F16
- F17
- M19
- M20
- M17
- M18
- L19
- L20
- K19
- J19

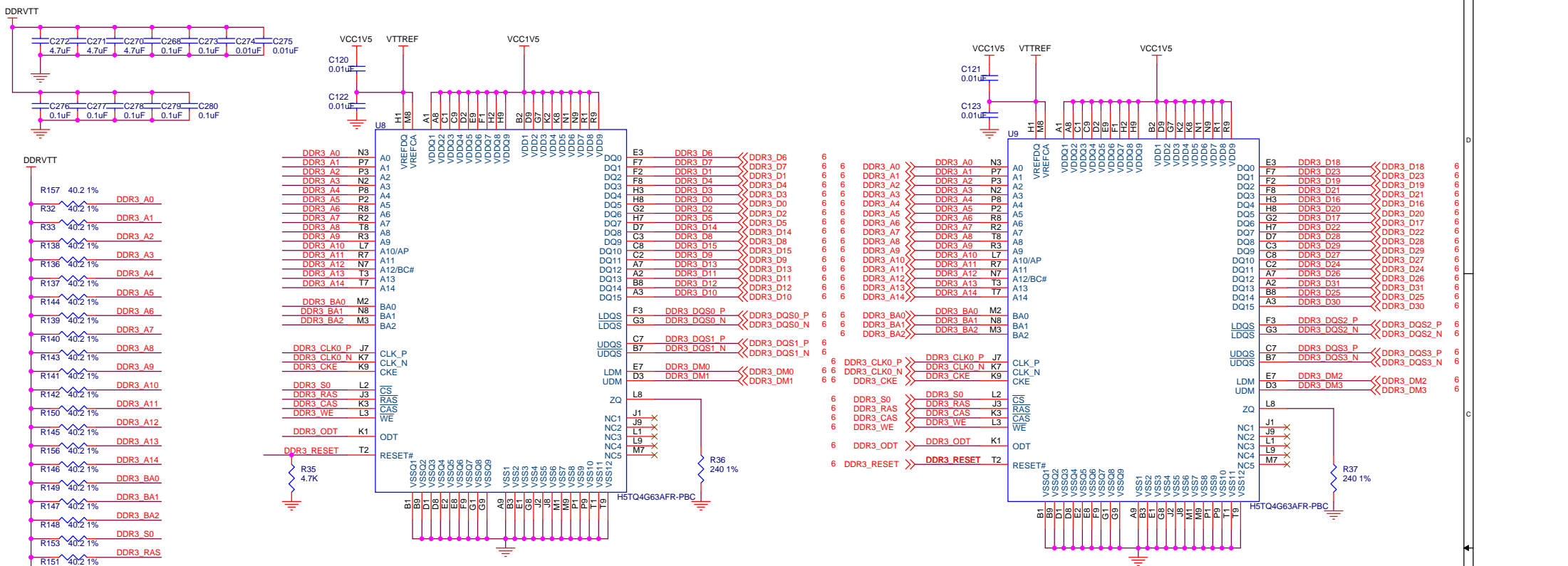


Zynq7010/7020

- L16
- L17
- K17
- K18
- H16
- H17
- J18
- H18
- F19
- F20
- G17
- G18
- J20
- H20
- G19
- G20
- H15
- G15
- K14
- J14
- N15
- N16
- L15
- M14
- M15
- K16
- J16
- IO2_10P
- IO2_10N
- IO2_7P
- IO2_7N
- IO2_15P
- IO2_15N
- IO2_4P
- IO2_4N
- IO2_2P
- IO2_2N
- IO2_14P
- IO2_14N
- IO2_9P
- IO2_9N
- IO2_3P
- IO2_3N
- IO2_16P
- IO2_16N
- IO2_17P
- IO2_17N
- KEY1
- KEY2
- RTC_DATA
- RTC_RESET
- LED1
- LED2
- LED3
- LED4







为了PCB走线方便, DDR3数据线组内 (DQS除外) 可以任意交换。
 XILINX 的UG933文档的PAGE66有以下说明:

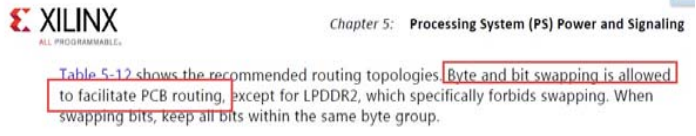
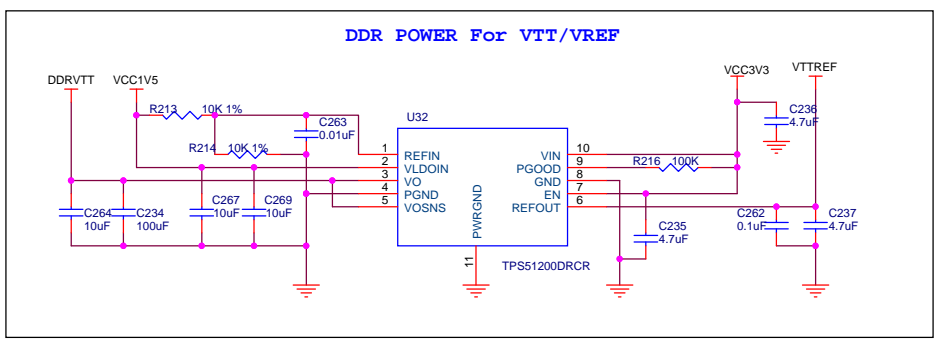
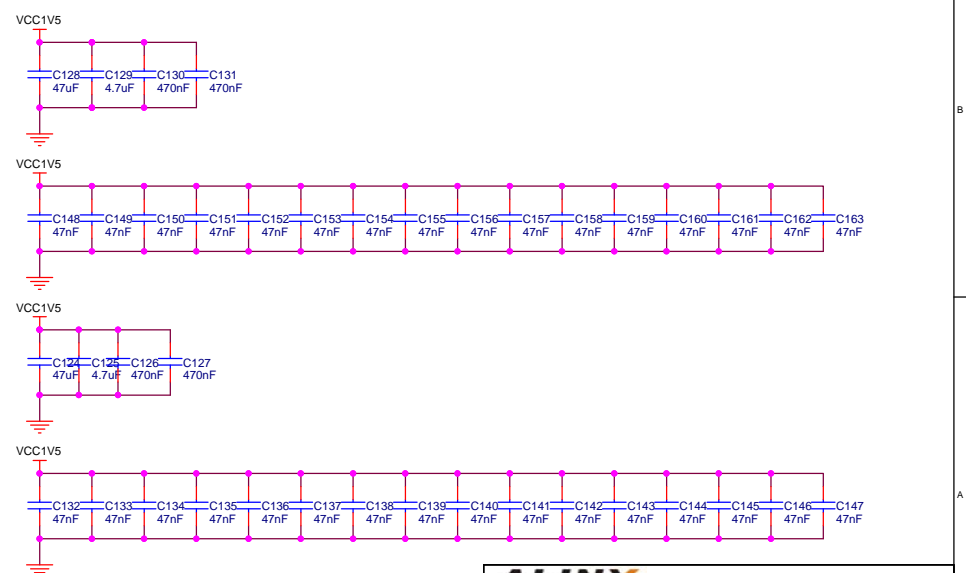
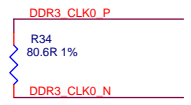
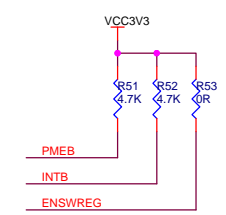
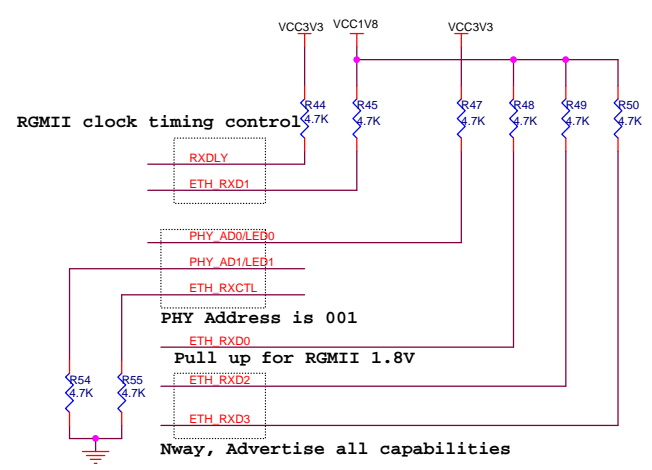
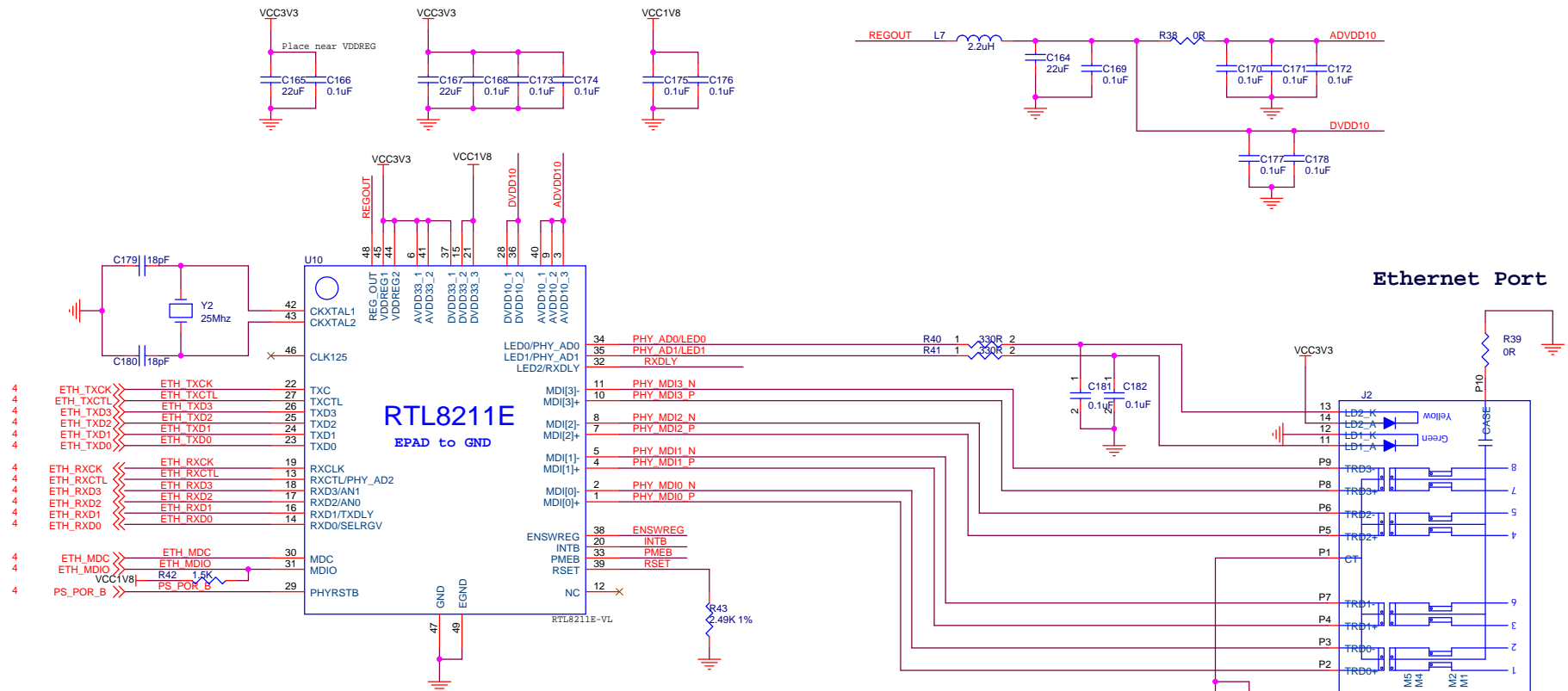
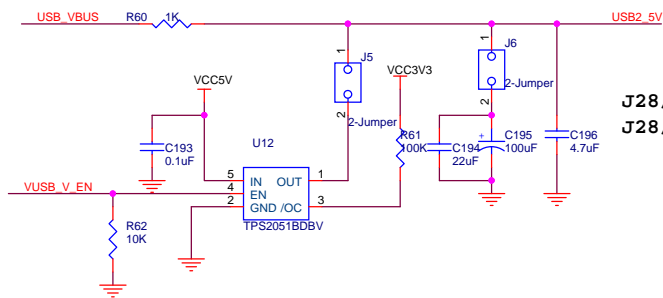
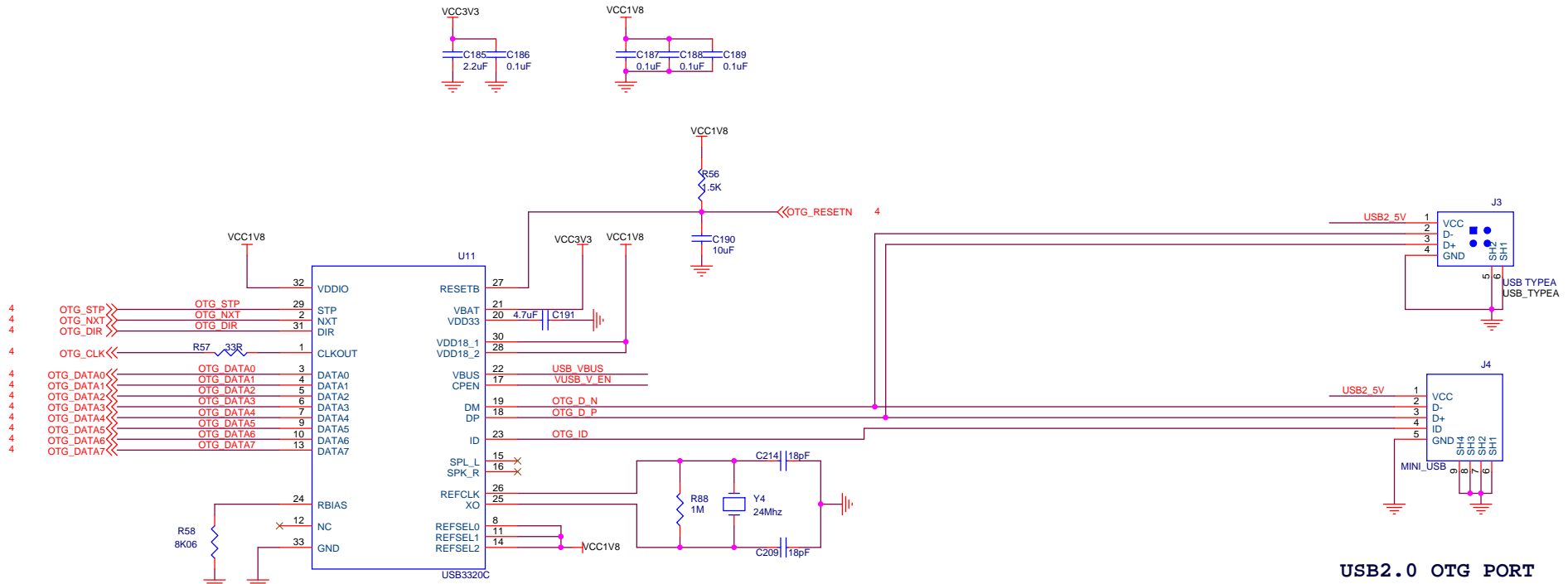


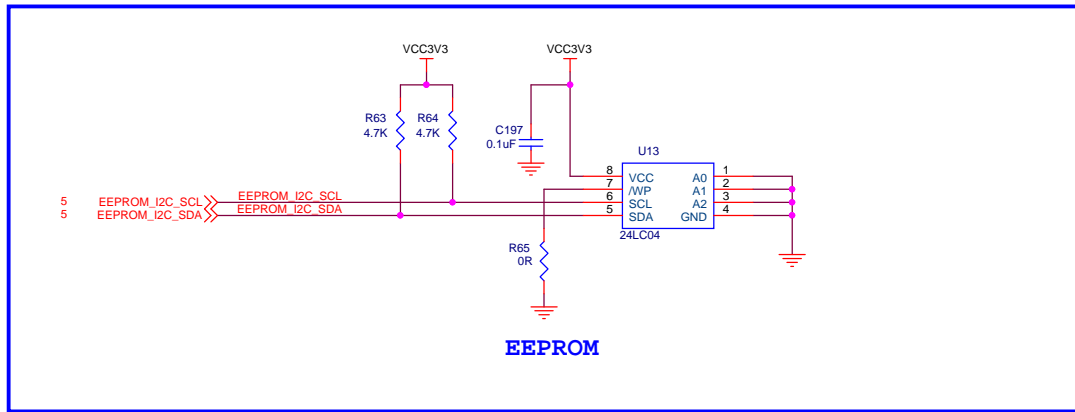
Table 5-12: DDR Routing Topology



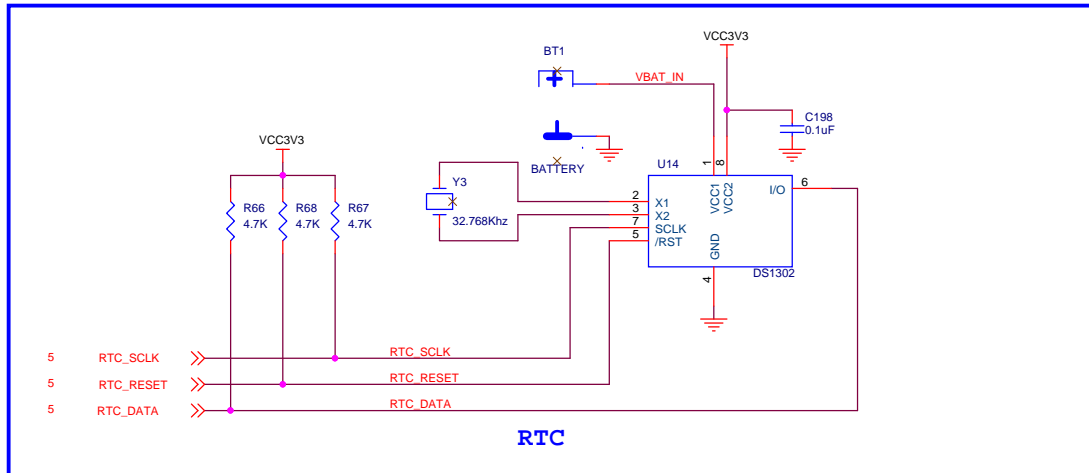




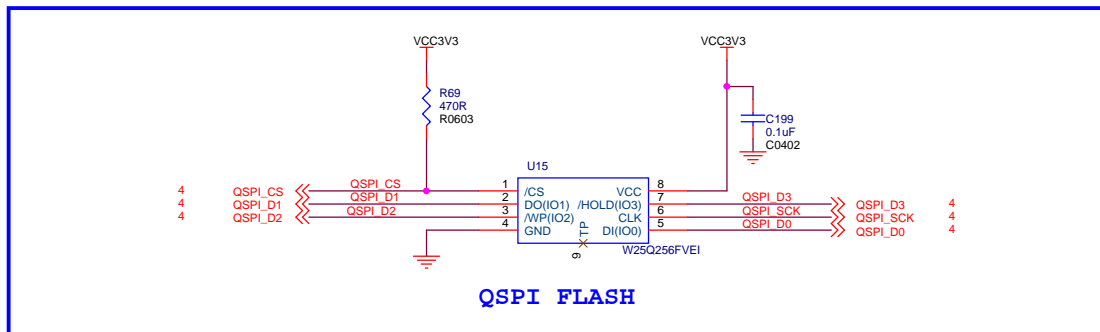
J28/J29 Connect: Host Mode
J28/J29 Not Connect: Slave/OTG Mode



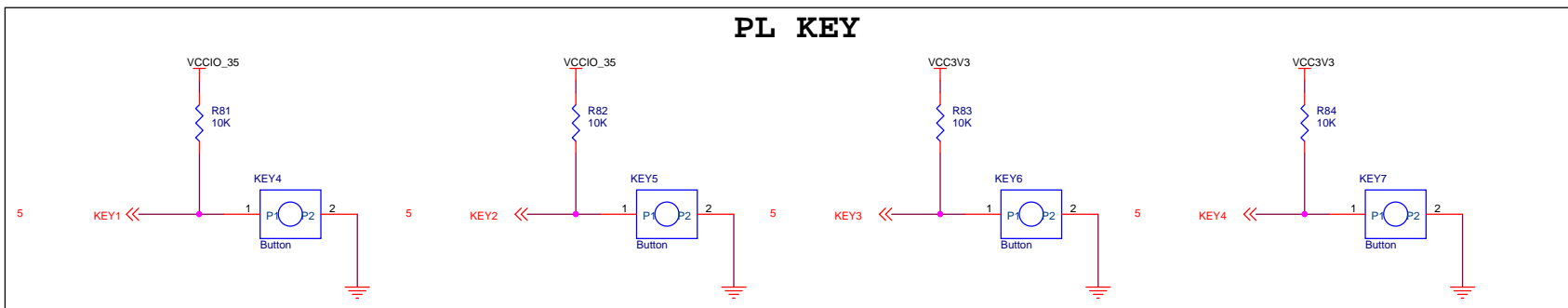
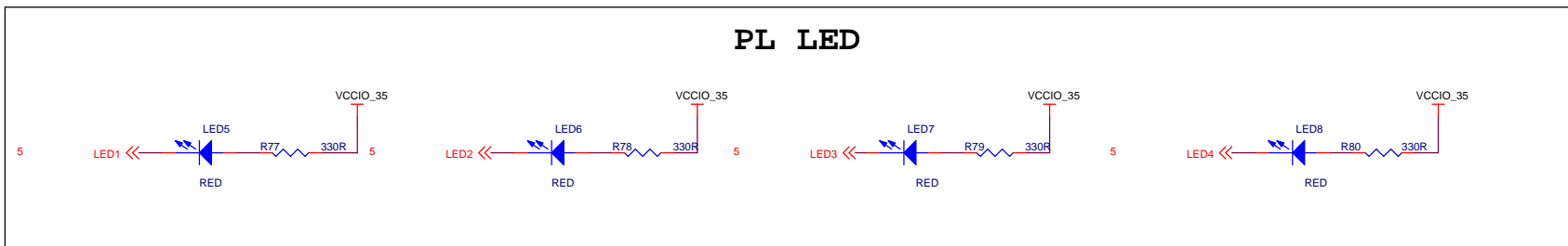
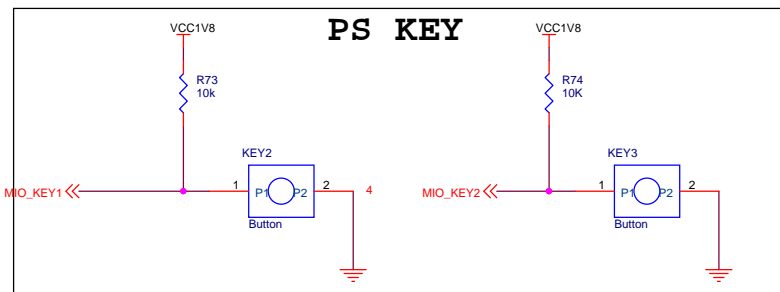
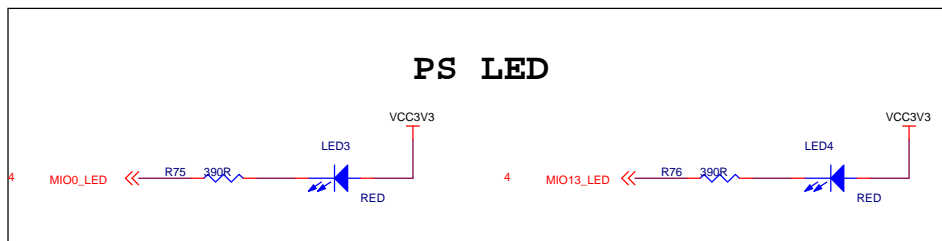
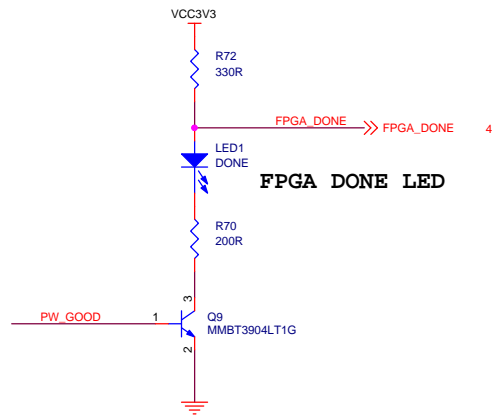
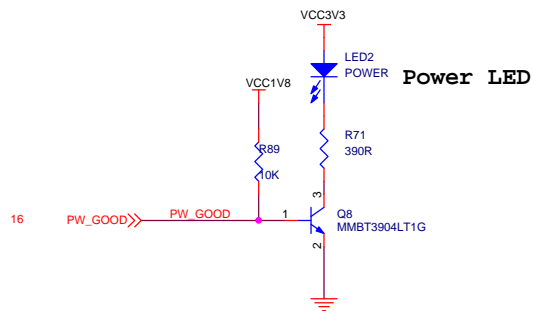
EEPROM



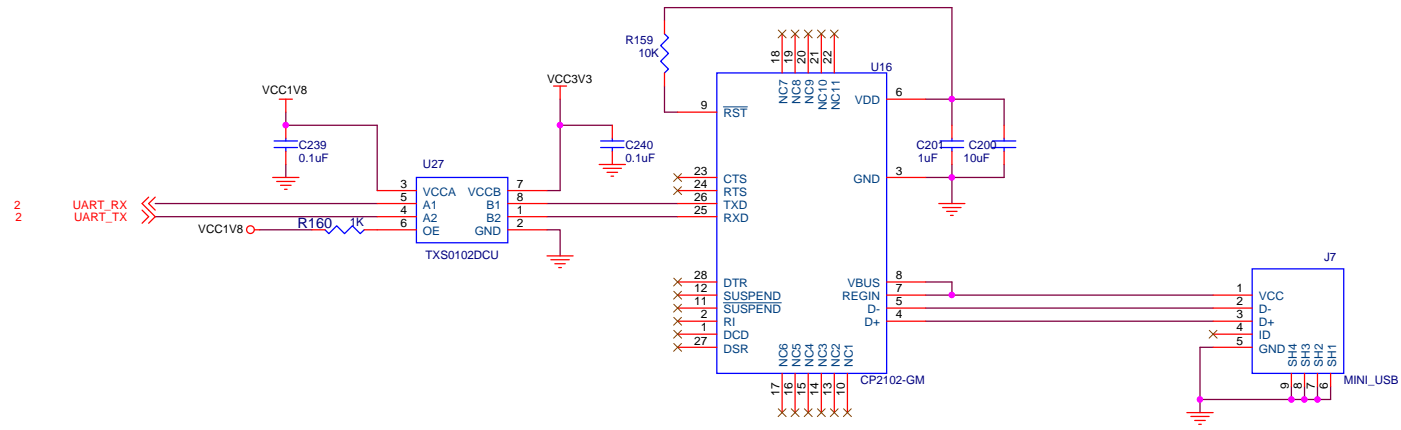
RTC



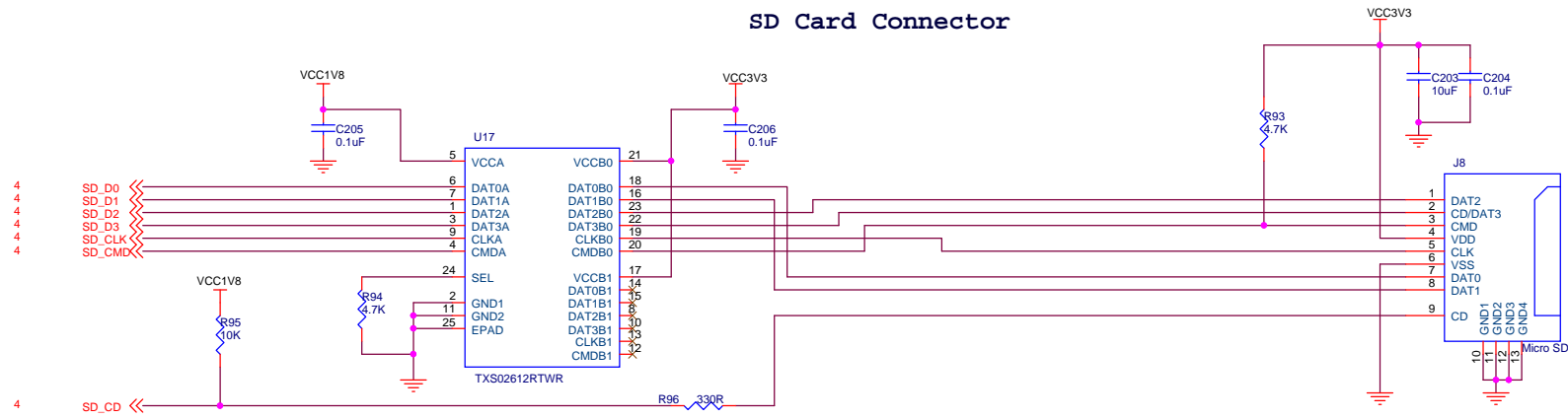
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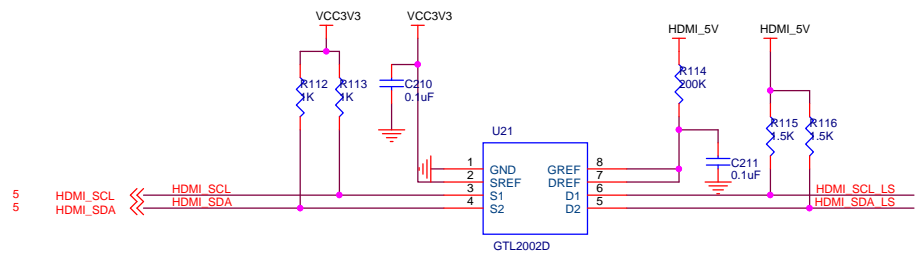
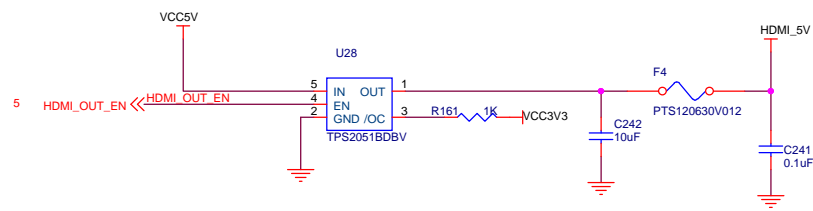
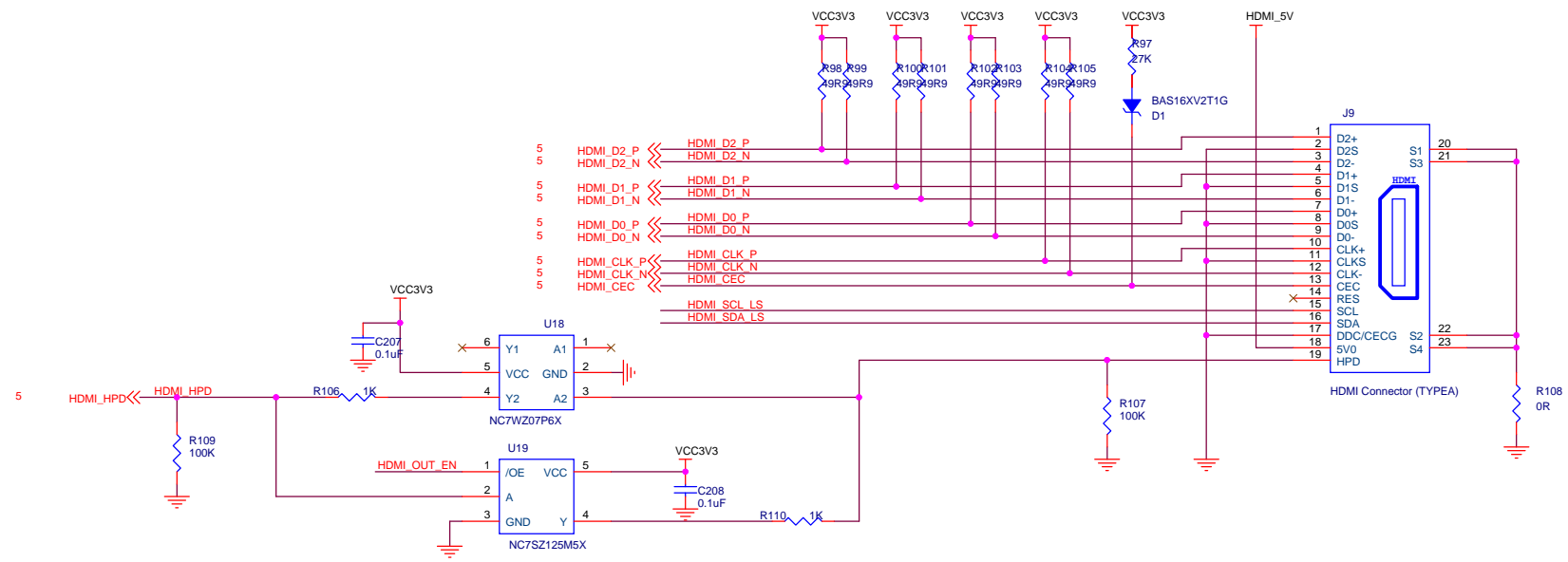


USB Uart

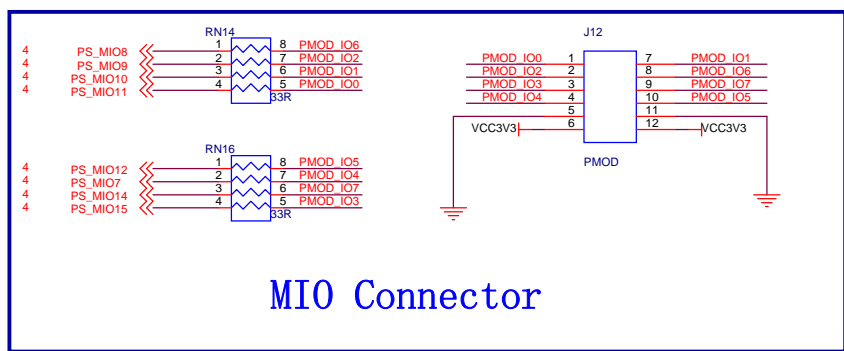
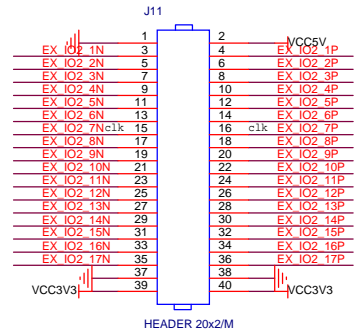
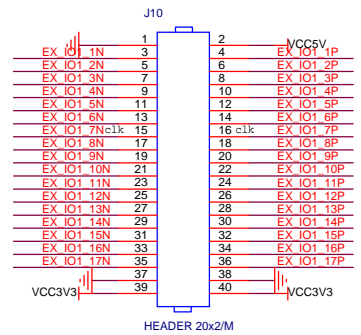
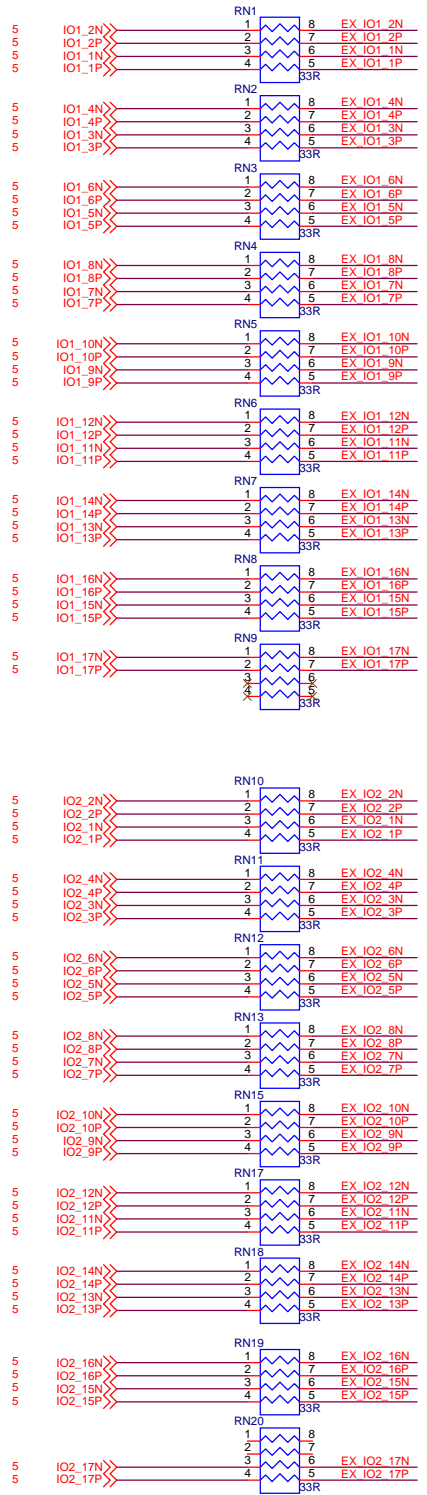


SD Card Connector



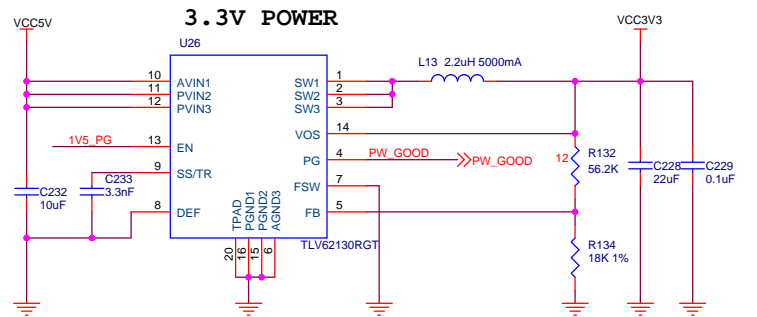
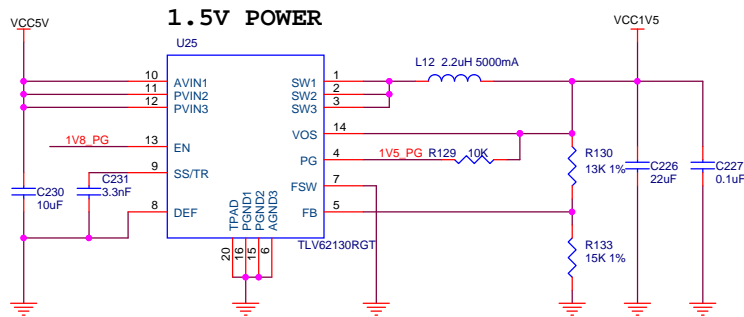
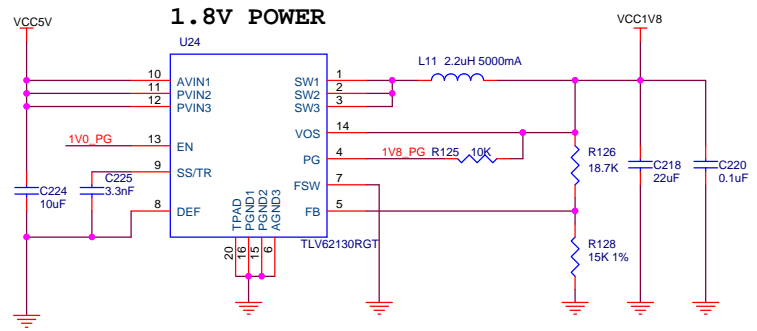
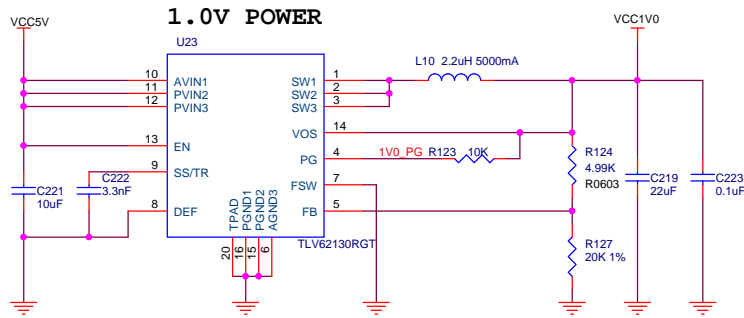
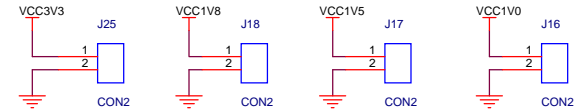
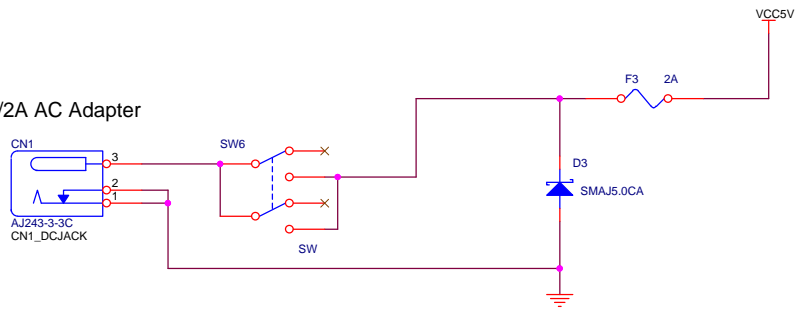


FPGA 40 PIN External IO



MIO Connector

5V/2A AC Adapter



Power On Sequence:

1.0V -> 1.8V -> 1.5V -> 3.3V -> VCCIO

